REVO WaRP Interposer Development Board User Guide
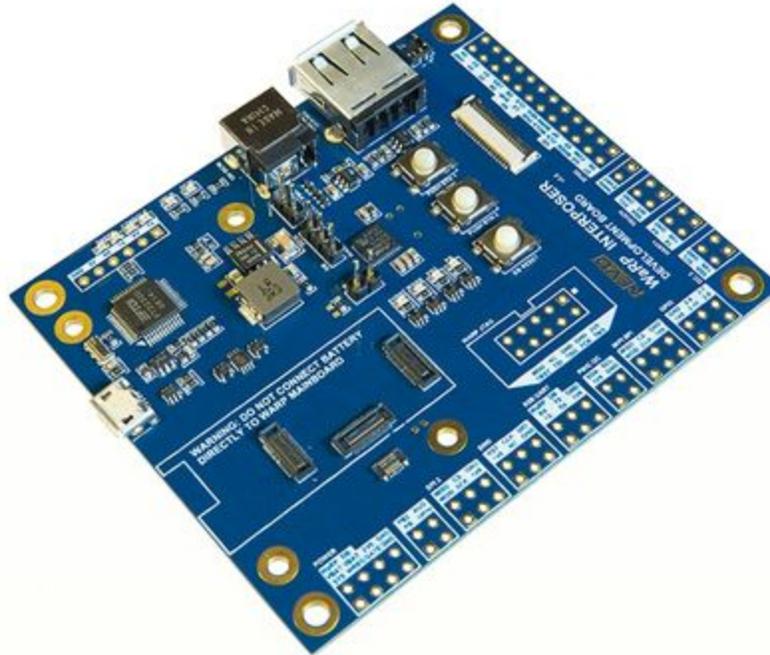
Document History

Revison	Date	
1.0	2014/12/21	Initial Release
2.3	2015/6/3	Update for interposer board v2.3 / v2.4
2.5	2015/8/23	Updated for IDB v2.5

Comments welcome! Any questions or comments are appreciated so that we can improve the community experience. Send us your feedback and will do our best to get a response to you quickly. Reach us via our website at revotics.com or email: support@revotics.com

Quick Setup Guide

Step 1. Attach WaRP and the display to the interposer (see Section 3 for details and jumper configuration).

Note: The default jumper configuration should be fine for most initial set ups.

Step 2. Attach a USB cable to the DEBUG micro-USB port on the Interposer and connect to your host computer.

Step 3. From your host computer, use a serial terminal application such as Putty to open up the serial console. The USB-UART will show two COM ports. The first is mapped to the Console (UART) of the WaRP and the second is used to monitor UART communication between WaRP and daughterboard. Typically the console is the higher numbered port associated with the USB-UART device.

Use the following settings: 115200 bps, 8-bits, No Parity, 1 Stop-bit (115200,8N1)

Windows: Open Device Manager and look under Ports for
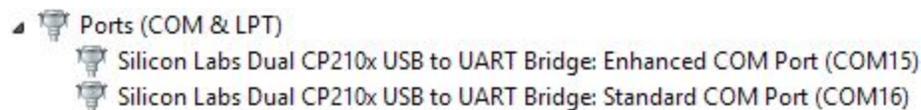
If no device show up, grab the driver from Silicon Lab's website: http://www.silabs.com

In Rev 2.3 and above, the ports should be named for easier identification.

Linux / Mac: Look for /dev/ttyUSB or /dev/tty.SLAB_USBtoUARTxx.

Use the screen, minicom, or similar to open a the uart.

Ex: $ screen /dev/tty.SLAB_USBtoUART2 115200

Step 4. Press the Power Button (PMIC PWR) to power on WaRP and you should see the U-Boot messages stream to the console.

1. Introduction

The WaRP Interposer Development Board was created to provide developers easy access to the various functions of WaRP. In addition to breaking out the pins, it also provides push buttons, LED indicators as well as access to both the serial console and UART B2B I/O via micro USB.

This board is also useful for software developers that need to work with the WaRP hardware, and need an easier way to handle the device.

To assist with development, daughterboards can be attached directly to the backside of the interposer. Additionally, the interposer provides the ability to bi-directionally inspect and inject UART communication between the mainboard and daughterboard to either device.

Board Features

● Ability to connect Mainboard and Daughterboard. Can be used to develop on either independently, or both simultaneously.

● Brings out most interfaces to standard (0.1″) pins

● Sturdy display mount. Touch panel can be used without the need for Daughterboard

● USB based serial console access

● Attach a battery or use an external power supply for continuous development

● Push buttons provided for development without daughterboard

● On-board regulators allow battery-less operation of WaRP, and charging of battery from DC supply.

Coming soon with firmware update:
● Monitor serial traffic between Mainboard and Daughterboard

● Status LED to show if connected battery level is too low

2. Interposer Pinout Overview

⚡ **Unless otherwise noted, signals to the WaRP Mainboard are at 1.8V. Application of higher voltages may cause permanent damage.**

(Unless otherwise noted, all signals are at 1.8V)

1 - POWER	
WaRP VBAT	WaRP Mainboard Postive Battery Terminal
DB VBAT	Daughterboard Positive Battery Terminal
SYS1	VSYS - Unregulated Primary System Voltage
2V9	2.9-3.2V - WaRP Mainboard VDD_HIGH
MB CHG	Mainboard Secondary Power Input
DB CHG	DB Output to WaRP Secondary Power Input
1V8	1.8V (Generated on Interposer)
GND	Ground

3 - SPI3			
MISO	IMX6SL	ECSPI3 MISO	(F15)
MOSI	IMX6SL	ECSPI3 MOSI	(D15)
CS	IMX6SL	ECSPI3 CS	(C22)
SCK	IMX6SL	ECSPI3 SCK	(F14)
1V8	1.8V	(Generated on Interposer)	
GND	Ground		

5 - B2B UART			
MB TX	IMX6SL	UART3 TX	(J21)
MB RX	IMX6SL	UART3 RX	(J19)
DB RX	KL16	UART1 RX	
DB TX	KL16	UART1 TX	
1V8	1.8V	(Generated on Interposer)	
GND	Ground		

7 - GPIO			
1-2	IMX6SL	GPIO_1_02	(J20)
1-3	IMX6SL	GPIO_1_03	(H20)
1-4	IMX6SL	GPIO_1_04	(H21)
1-5	IMX6SL	GPIO_1_05	(J22)
1-17	IMX6SL	GPIO_1_17	(G16)
1-19	IMX6SL	GPIO_1_19	(D14)
1-20	IMX6SL	GPIO_1_20	(B14)
1-21	IMX6SL	GPIO_1_21	(A14)
1-22	IMX6SL	GPIO_1_22	(A13)
1-23	IMX6SL	GPIO_1_23	(B10)
1V8	1.8V	(Generated on Interposer)	
GND	Ground		

9 - UART1		
TX	IMX6SL Console UART1 TX	(D19)
RX	IMX6SL Console UART1 RX	(B19)

10 -TOUCH			
2V9	2.9-3.2V - WaRP Mainboard VDD_HIGH		
1V8	1.8V	(Generated on Interposer)	
SDA	IMX6SL (D18)	I2C2 SDA	
SCL	IMX6SL	I2C2 SCL	(E18)
INT	IMX6SL	GPIO_2_12	(F10)
GND	Ground		

11 - CONTROL			
WAKE	IMX6SL	GPIO_5_14	(B21)
EVNT	IMX6SL	GPIO_5_11	(B23)

2 - Push Buttons			
PB	PMIC Button PMIC Power Control		
PB2	IMX6SL Button GPIO_5_15		(B20)

4 - DB SWD			
SWD_RST#	IMX6SL	GPIO_3_31	(E21)
SWD_CLK	IMX6SL	GPIO_5_08	(A23)
SWD_DIO	IMX6SL	GPIO_5_06	(B22)
32KHz	PMIC 32.768KHz Clock Output		
1V8	1.8V	(Generated on Interposer)	
GND	Ground		

6 - PMIC I2C			
SDA	IMX6SL	I2C1 SDA	(AD13)
SCL	IMX6SL	I2C1 SCL	(AC13)
1V8	1.8V	(Generated on Interposer)	
GND	Ground		

8 - I2C3			
SDA	IMX6SL	I2C3 SDA	(A9)
SCL	IMX6SL	I2C3 SCL	(B9)
1V8	1.8V (Generated on Interposer)		
GND	Ground		

12 - EPDC			
D0	IMX6SL	EPDC_D0	(A18)
D1	IMX6SL	EPDC_D1	(A17)
D2	IMX6SL	EPDC_D2	(B17)
D3	IMX6SL	EPDC_D3	(A16)
D4	IMX6SL	EPDC_D4	(B16)
D5	IMX6SL	EPDC_D5	(A15)
D6	IMX6SL	EPDC_D6	(B15)
D7	IMX6SL	EPDC_D7	(C15)
GG	PMIC	VEPD_GG	**(+22V)**
COM	PMIC	VEPD_COM	**(-1V)**
MODE	IMX6SL	EPDC_GDOE	(B13)
EE	PMIC	VEPD_EE	**(-20V)**
GDCLK	IMX6SL	EPDC_GDCLK	(A12)
GDSP	IMX6SL	EPDC_GDSP	(A11)
MCLK	IMX6SL	CSI_MCLK	(B12)
BDR	Analog output based on BDR[1:0] selection		
POS	PMIC	VEPD_POS	**(+15V)**
NEG	PMIC	VEPD_NEG	**(-15V)**
SDLE	IMX6SL	EPDC_SDLE	(B8)
SDCLK	IMX6SL	EPDC_SDCLK	(B10)
SDSHR	IMX6SL	EPDC_SDSHR	(F7)
SDOE	IMX6SL	EPDC_SDOE	(E7)
SDCE0	IMX6SL	EPDC_SDCE0	(C11)
GND	Ground		

3. Setup Overview

Attaching the WaRP Mainboard to the Interposer

WaRP uses three (3) board-to-board connectors for its IO as described above. It is important to note that improper attachment/removal can damage these connectors. Always attach and detach the board vertically. Please review the following excerpt from Hirose DF40 Datasheet.

Handling Precautions when mating the connectors
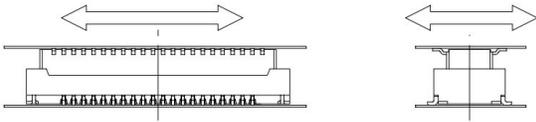
	Keep the connectors parallel to each other when positioning
	Do not attempt to mate the connectors staring at one end or side.
	Press-down evenly until slight resistance is felt. Overcoming this slight resistance will complete the mating receptacle with the header. A definite "click" sensation will confirm the fully mated condition.
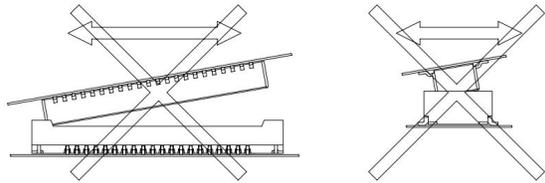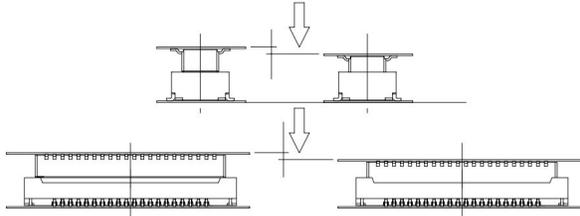
Align the WaRP Mainboard connectors with the Interposer connectors on the top and make sure there are no obstructions. Press down gently until the board clicks in. Check to ensure that the board is firmly seated on the Interposer and that the Mainboard is parallel to the Interposer.

Note: Depending on the application, not all ports may be present. For example, minimal functionality can be achieved by only using one (1) board-to-board connector. In setups that require all three, the mating force may be significant if the connectors are not properly aligned on the boards.
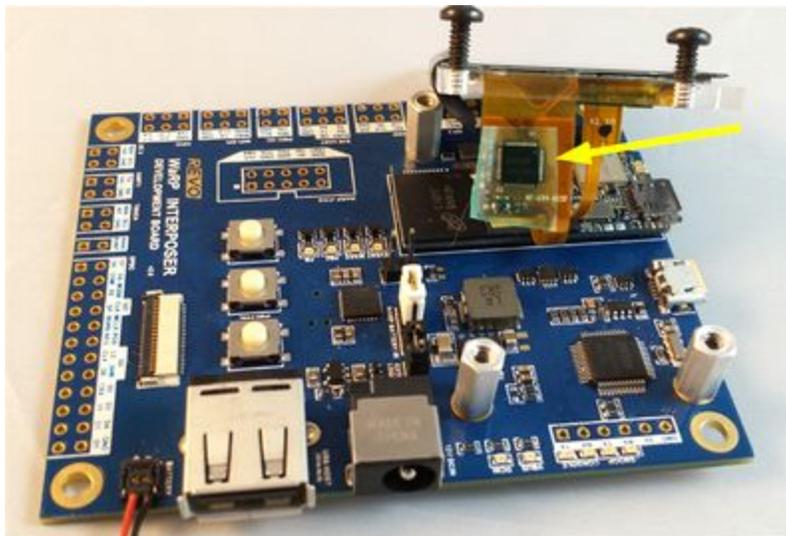
Attaching the Display

For peripherals, additional small-pitch connectors are used. The display and touch panel are split into two separate connectors to maximize compatibility. Review the images below to ensure that the display connectors are attached in the proper orientation. Connecting the display or touch panel in the wrong orientation may damage the device.

The flex cables have a reinforced backing on both the display and touch connectors. The reinforced area allows for safe handling. Do not tug or pull on the unsupported flex cables as it may damage the wiring in the cables.

Display and touch connector orientation

If the touch controller is not encapsulated, cover exposed contacts with electrical tape to avoid shorting to WaRP.

The Interposer ships with a display stand allow the display to be attached to the Interposer securely. Attach the display to the display stand using the tape adhesive on the back on the display. If your display does not have the tape adhesive, you can use any kind of take to secure the edge of the display to the display stand. Thinner tapes work best so they do not interfere with the touch panel.

Attaching the Daughterboard

The daughter board can be attached to the bottom side of the Interposer. This is especially useful as the signals going between the boards can be inspected and monitored for development purposes.

Following the same procedure as attaching the Mainboard, align the Daughterboard connector to the bottom of the Interposer, and press gently in a vertical manner. The Daughterboard should click in.

4. Board Function Details

Interposer Block Details

Power (Callout 1)

>**WaRP VBAT**
>VBAT input to WaRP mainboard. This node connects to the WaRP mainboard PMIC providing power and charge path. This path can be connected to a battery or a emulated, regulator generated battery voltage via the **WARP BATTERY IN (15)** header.
>
>**DB VBAT**
>Interposer battery voltage supplied either as an emulated battery voltage from a 4.1V regulator or through the interposer **BATTERY (14)** connector.

PB (Callout 2)

>Breakout of the power button and push button 2 signals.

SPI3 (Callout 3)

>User accessible breakout of i.MX6SL SPI3 for development and connection of SPI peripherals.

DB SWD (Callout 4)

>SWD connections for debug and programming KL16 of Pedometer daughterboard.

B2B UART (Callout 5)

>This UART is the dedicated (primary) communication channel between the WaRP Mainboard and daughterboards. This port is reserved for board to board communication usage under the Hybrid Design Architecture.

PMIC I2C (Callout 6)

>Note: Disconnected on Interposers version 2.3.
>
>This connects directly to the I2C interface of the PMIC and should only be used for advanced configuration purposes. This channel should **not** be used to connect peripherals.

GPIO (Callout 7)

>Note that many of the other ports also have alternate pin functionality as GPIO.
>Alternate configuration of these GPIO pins provides access to i.MX6SL AUD_MUX

I2C3 (Callout 8)

>User accessible breakout of i.MX6SL I2C3 for development and connection of I2C peripherals. For I2C operation, external pull-ups must be supplied by the attached device or enabled in the WaRP kernel pad configuration if the available internal i.MX6SL pull-up values are acceptable for the

application.

UART1 (Callout 9)

Connected to the Console of WaRP. This interface is monitored via the Interposer's onboard UART-USB.

TOUCH (Callout 10)

SCL, SDA, and INT signals on this Touch block (block 11) connect directly to the i.MX6SL I2C2 interface and GPIO respectively. By default they are used exclusively for the touch screen.

The i.MX6SL I2C2 SCL and SDA pads are configured as open drain with 22K on-chip pull-ups enabled on the 1.8V VDD_LOW domain. INT is by default configured as a GPIO input on the VDD_LOW (1.8V) i.MX6SL voltage domain.

CONTROL (Block 11)

Breakout of GPIO signals connected between Pedometer daughterboard KL16 and i.MX6SL providing power management control signals.

EPDC (Callout 12)

Provides breakout access to EPDC connections.

Jumper J8 / LOAD

This jumper is used to recover the firmware on the Interposer. Keep this disconnected unless your Interposer needs to be updated with new firmware.

Jumper J9 / SYS1 Power to 1V8 Regulator VIN

This jumper is used to connect SYS1 from WaRP to power the 1.8V regulator on the Interposer. This is useful as it allows just one USB cable (attached to WaRP) to power everything. However, the Interposer draws power from this 1.8V as well so this is not ideal for making power measurements. If this jumper is removed make sure that either the USB Debug Power jumper is connected, or 12V DCIN is supplied.

Jumper BM

Close this jumper to pull BOOT_MODE0 high and force serial bootloader mode on reset. Only use this if you need to force the i.MX6 into the serial bootloader. Default: Open

Jumper ALT CHARGE SOURCE

Jumper selects between the daughterboard wireless charging output or a 6.1V regulated voltage generated from the the 12V DC input on the interposer as the alternate charge input on WaRP.

Selecting DCIN allows the battery to charge from the Interposer 12V DC input.

Selecting DB allows the battery to be charged from the wireless charger on the pedometer daughterboard.

Default: DCIN

Jumper WARP BATTERY SOURCE

Jumper selects whether VBATT is provided to mainboard from battery or derived from the Interposer power source (12V DC or USB-UART).

Selecting DCIN allows battery-less operation of WaRP. Note that WaRP will see this as ~4.1V input on VBAT to simulate the battery.

Selecting DB allows operation of WaRP from battery connected to the Interposer or a daughter board attached to the bottom of the interposer. This also allows for charging of the battery.

Default: DCIN

USE DEBUG POWER

When jumpered, the interposer can derive its power from UART-USB connection. If a 12V adapter is connected to DCIN, this jumper can be removed so that power to the board is supplied via the adapter.

Default: On / Jumpered

DCIN

Connect an optional 12V adapter. Needed only if too much power is being drawn via the DEBUG USB interface from your host computer, and/or if you wish to operate WaRP without a battery.

Power Button / PB1

Holding down for 12 seconds forces PMIC to power cycle. Once u-boot has loaded this delay is reduced to 2s for development convenience. If in 'factory ship mode' this will trigger a reset. If not in factory ship mode this will power up/down the unit.

Push Button 2 / PB2

This provides a general purpose push button and is connected to GPIO on both the WaRP mainboard i.MX6SL and the Pedometer Daughterboard KL16.

DB Reset Button

Active low reset signal to KL16 on the Pedometer daughterboard.

USB Host

When Interposer is powered from 12V, the USB A connector may be used to access USB host mode functionality of the i.MX6SL, allowing for USB peripherals to be connected to WaRP.

DB Battery

Battery connector for powering WaRP.

Status LED is ON when a battery under-voltage condition has been detected.

JTAG

0.1" 2x5 JTAG header for debug of the i.MX6SL on WaRP mainboard.

DB SWD

0.05" 2x5 SWD header for debug and programming KL16 on Pedometer daughterboard.

5. Mechanical Drawing

Notice of Disclaimer

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