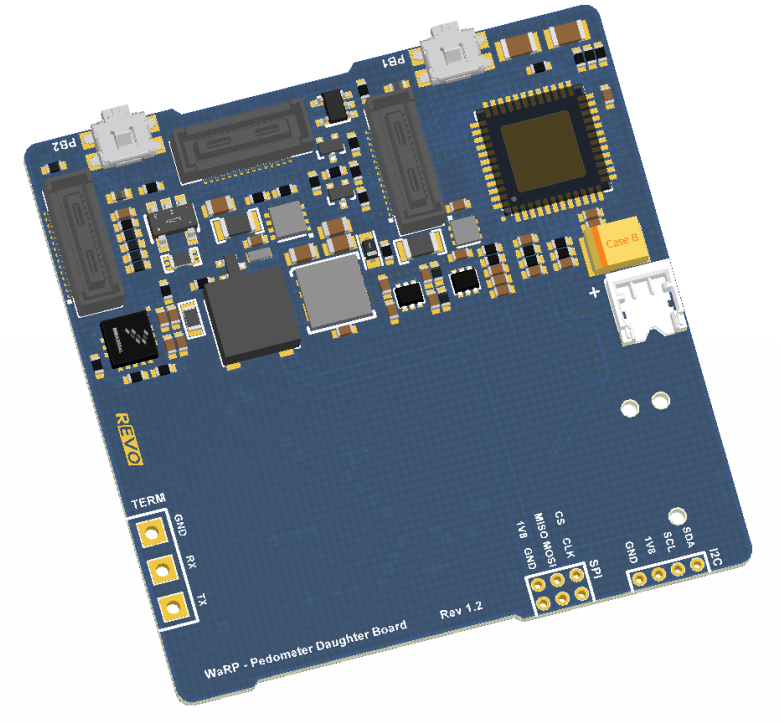

WaRP Daughterboard

Design Quicksheet

Document Revision: 1.5 (May 11, 2015)
Written and maintained by Revolution Robotics

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Document History

Revison	Date	
1.0	2014/5/22	Initial internal release
1.5	2015/5/11	Initial public revision

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Table of Contents

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Overview of Available WaRP Board-to-board Interfaces

- 2x UART
- 3x I2C
- 4-bit SPI to AP
- Up to 52x GPIO to AP
- USB Host
- Audio
- Electronic Paper Display Interface
- JTAG interface to AP
- VBAT Input
- Boot Mode override
- Secondary Charger Input
- 32.768 kHz clock
- PMIC for RTC, power and battery management

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Electrical Guidelines

Absolute Maximum Electrical Characteristics

WaRP Secondary Charger Input Voltage	-0.3V to +16V
Input voltage from Mainboard	-0.3V to +6V

Electrical Characteristics

	Min	Typical	Max
Input Voltage from Mainboard (SYS_PWR)	2.7V	4V	5.5V
Secondary Charger Voltage Output to WaRP Mainboard	6.2V	5V	6.3V (operating) 16V (tolerant)
WaRP Mainboard IO signal [1]		1.8V	
VBAT	2.7V		4.2V

[1] signal voltages of the WaRP Mainboard default to 1.8V. 3V signaling requires kernel customization.

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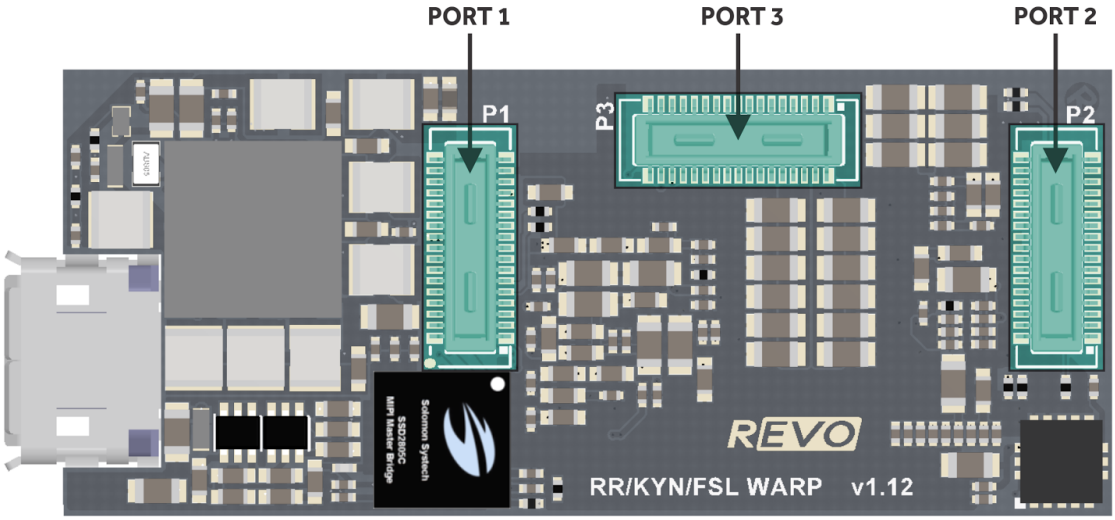
Pin Map & Pin Function Description

WaRP Mainboard I/O Connectors



WaRP Mainboard (Bottom View)

Connector Port 1 (Nearest USB)

PWR Control - Wake/Push Button/Event triggers
UART - Board to Board Communication
PMIC_CTL - I2C interface for interfacing to PMIC (multi master)
SPI3 - i.MX6 SPI3 interface available for application peripherals
VBAT - Connection to battery attached to daughterboard
VSYS_PWR - Power from PMIC to power daughterboard
ALT_CHARGE - Secondary charger input from daughterboard (Wireless Charging)
32K_CLK - 32.768K Clock maintained by mainboard for use by MCU on DB
GPIO - i.MX6 GPIO available for power management and application peripherals

Connector Port 2 (Furthest from USB)

JTAG - i.MX6 JTAG interface
UART - i.MX6 UART1 serial console access
USB - i.MX6 USB interface
I2C3 - i.MX6 I2C3 interface available for application peripherals
AUD3 - i.MX6 AUD_MUX interface available for application audio peripherals
GPIO - i.MX6 GPIO available for and application peripherals

Connector Port 3 (Middle)

E-Paper Display - i.MX6 EPDC interface ([0:7] on Port 3, [8:11] on Port 2, [12:15] on Port 1)
Touch Panel Interface - i.MX6 I2C2 interface configured for touch panel by default

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Connector Port 1

PIN	NAME	Function	Notes
1	GND	Ground	
2	GND	Ground	
3	GND	Ground	
4	I2C1_SCL	iMX6SL I2C1_SCL	Additional I2C devices or PMIC control
5	I2C1_SDA	iMX6SL I2C1_SDA	Additional I2C devices or PMIC control
6	GPIO5_8	WaRP GPIO/KL16 SWD_CLK	SD1_DAT1
7	UART3_TXD	iMX6SL UART3_TX, KL16 UART0_RX	WaRP to DB UART, AUD3_RXFS
8	UART3_RXD	iMX6SL UART3_RX, KL16 UART0_TX	WaRP to DB UART, AUD3_RXC
9	GPIO5_6	WaRP GPIO	SD1_DAT3
10	GPIO3_31	WaRP GPIO	
11	ECSPI3_SCLK	iMX6SL SPI3/EPDC/GPIO	
12	ECSPI3_MOSI	iMX6SL SPI3/EPDC/GPIO	
13	ECSPI3_MISO	iMX6SL SPI3/EPDC/GPIO	
14	GPIO5_13	iMX6SL SPI3/GPIO	SD1_DAT2
15	GND	Ground	
16	ECSPI3_SS0	iMX6SL EPDC/GPIO	GPIO1_17
17	CTRL_EVENT	WaRP B2B power management	SD1_DAT0
18	PMIC_32K_CLK	32.768 KHz clock	
19	CTRL_WAKE	WaRP B2B power management	SD1_CMD
20	CTRL_PB2	General purpose button	SD1_CLK
21	B2B_PMIC_PB	Multifunction power button	
22	DB_ALT_CHRG	WaRP secondary charger input	ALT charger input to the WaRP PMIC
23	DB_ALT_CHRG	WaRP secondary charger input	ALT charger input to the WaRP PMIC
24	VSYS_PWR	WaRP system power output	Source for all downstream regulators
25	VSYS_PWR	WaRP system power output	Source for all downstream regulators
26	VBAT	WaRP battery input	
27	VBAT	WaRP battery input	
28	VBAT	WaRP battery input	
29	VBAT	WaRP battery input	
30	VBAT	WaRP battery input	

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Connector Port 2

PIN	NAME	Function	Notes
1	UART1_RXD	iMX6SL UART1_RX serial console	
2	UART1_TXD	iMX6SL UART1_TX serial console	
3	JTAG_TRSTB	i.MX6SL JTAG	VDDH (2.9V-3.2V) domain
4	JTAG_TDI	i.MX6SL JTAG	VDDH (2.9V-3.2V) domain
5	JTAG_TMS	i.MX6SL JTAG	VDDH (2.9V-3.2V) domain
6	JTAG_TCK	i.MX6SL JTAG	VDDH (2.9V-3.2V) domain
7	JTAG_TDO	i.MX6SL JTAG	VDDH (2.9V-3.2V) domain
8	JTAG_MOD	i.MX6SL JTAG	VDDH (2.9V-3.2V) domain
9	USB_HOST_D_P	USB_OTG2_DP	
10	USB_HOST_D_N	USB_OTG2_DN	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	GND	Ground	
16	I2C3_SDA	iMX6SL I2C/GPIO	
17	I2C3_SCL	iMX6SL I2C/GPIO	
18	GPIO1_5	iMX6SL AUD3/GPIO	
19	GPIO1_4	iMX6SL AUD3/GPIO	
20	GPIO1_3	iMX6SL AUD3/GPIO	
21	GPIO1_2	iMX6SL AUD3/GPIO	
22	GND	Ground	
23	GND	Ground	
24	EPDC_D15	iMX6SL EPDC/UART2/GPIO	
25	EPDC_D14	iMX6SL EPDC/UART2/GPIO	
26	EPDC_D13	iMX6SL EPDC/UART2/GPIO	
27	EPDC_D12	iMX6SL EPDC/UART2/GPIO	
28	V2P9	WaRP V2P9 supply output	WaRP VDDH (2.9V-3.2V)
29	BOOT_MODE0	iMX6SL BOOT_MODE selection	Force serial bootloader
30	GPIO4_23	iMX6SL GPIO	

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Connector Port 3

PIN	NAME	Function	Notes
1	GND	Ground	
2	TOUCH_INT	LCD Touchpanel Interface Interrupt	
3	EPDC_GDRL	EPDC Signal	
4	TOUCH_SDA	LCD Touchpanel Interface	
5	TOUCH_SCL	LCD Touchpanel Interface	
6	EPDC_BDR0	EPDC Signal	
7	EPDC_GDCLK	EPDC Signal	
8	EPDC_GDSP	EPDC Signal	
9	MODE	EPDC Signal	
10	VEPD_EE	EPDC Supply	-20V
11	VEPD_GG	EPDC Supply	22V
12	VEPD_COM	EPDC Supply	VCOM
13	EPDC_BDR1	EPDC Signal	
14	EPDC_D7	EPDC Signal	
15	EPDC_D6	EPDC Signal	
16	EPDC_D5	EPDC Signal	
17	EPDC_D4	EPDC Signal	
18	EPDC_D3	EPDC Signal	
19	EPDC_D2	EPDC Signal	
20	EPDC_D1	EPDC Signal	
21	EPDC_D0	EPDC Signal	
22	EPDC_SDCE0	EPDC Signal	
23	EPDC_SDSHR	EPDC Signal	
24	EPDC_SDOE	EPDC Signal	
25	EPDC_SDLE	EPDC Signal	
26	EPDC_SDCLK	EPDC Signal	
27	V2P9	WaRP V2P9 supply output	WaRP VDDH (2.9V-3.2V)
28	GND	Ground	
29	VEPD_POS	EPDC Supply	15V
30	VEPD_NEG	EPDC Supply	-15V

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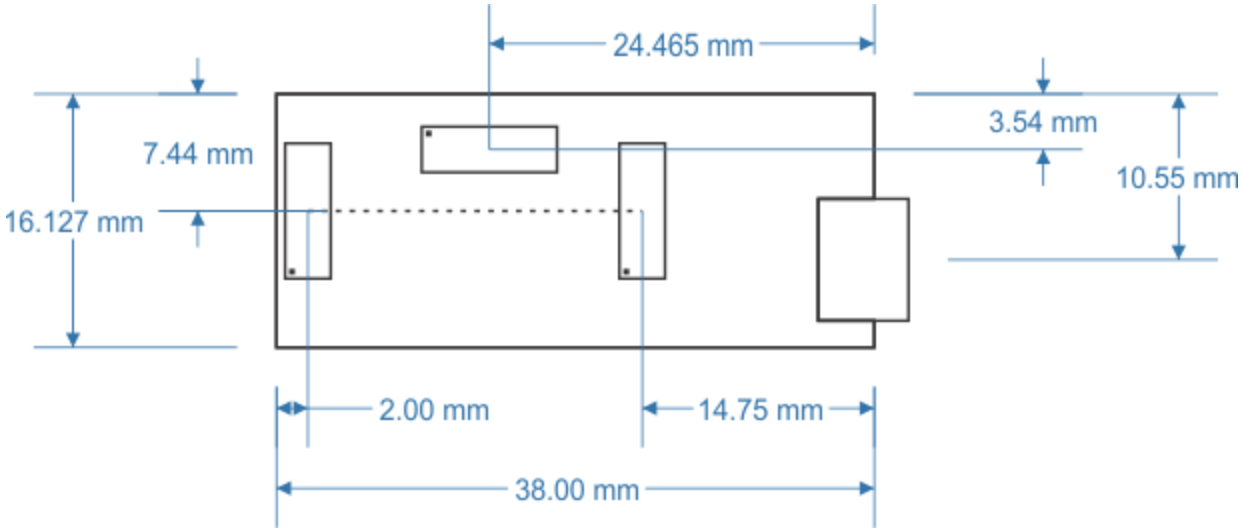
Mechanical Design Guidelines

Board-to-Board Connectors

The WaRP Mainboard uses three (3) identical 30-pin board-to-board connectors. These connections are all on the bottom side of the mainboard.

WaRP Mainboard (Bottom View)



Mating Connector to use on Daughterboard:
DF40HC(3.0)-30DS-0.4V(51) - Hirose 30 pin 0.4 pitch 3.0mm receptacle

Component Clearance

The WaRP Mainboard is a densely populated board with components residing on both sides of the PCB. The tallest component on the bottom side of the board is 1.2mm from the bottom of the PCB. The Hirose DF40 series of connectors used on this platform have several variants for different mated heights. We recommend and utilize the 3mm mated height to allow for parts to be placed under the mainboard area of the daughterboard.

Consideration is recommended to avoid thermal and EMI conflicts with mainboard components.

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Power Design Guidelines

VSYS_PWR is provided by the PMIC on the WaRP Mainboard. DO NOT CONNECT TO A POWER SOURCE. DO NOT CONNECT THIS PIN TO ANOTHER POWER RAIL.

Battery connection

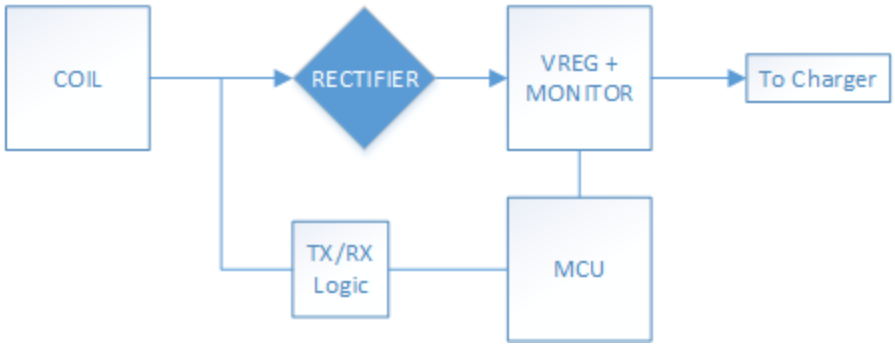
While a battery can be directly soldered to the WaRP mainboard it is generally desirable to provide a battery connector on the daughterboard to allow for a removeable battery. The battery terminal voltages are connected to the PMIC on the mainboard for fuel gauge monitoring and voltage regulation through the board to board connectors. While this configuration allows the battery to be connected to daughterboard, it should not be used to power the daughterboard components directly as this will prevent the PMIC from monitoring and charging safely.

System Voltage

The WaRP Mainboard provides VSYS_PWR, a monitored system voltage from the PMIC from which the daughterboard should derive its supply. Typical daughterboards should operate at 1.8V unless mainboard kernel modifications are made to adjust IO voltages. A high efficiency switching regulator to generate 1.8V from VSYS_PWR is recommended.

Wireless charging

The DB_ALT_CHRG input is where power should be supplied from an alternate charging source such as a wireless charger. Although the input is tolerant up to 16V, the charger is only active when the voltage is between 3.2V and 6.3V. For wireless charging this is accomplished by adding an intermediary 5V regulator to the output of rx coil.



Qi Charger block diagram as implemented on pedometer daughterboard

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