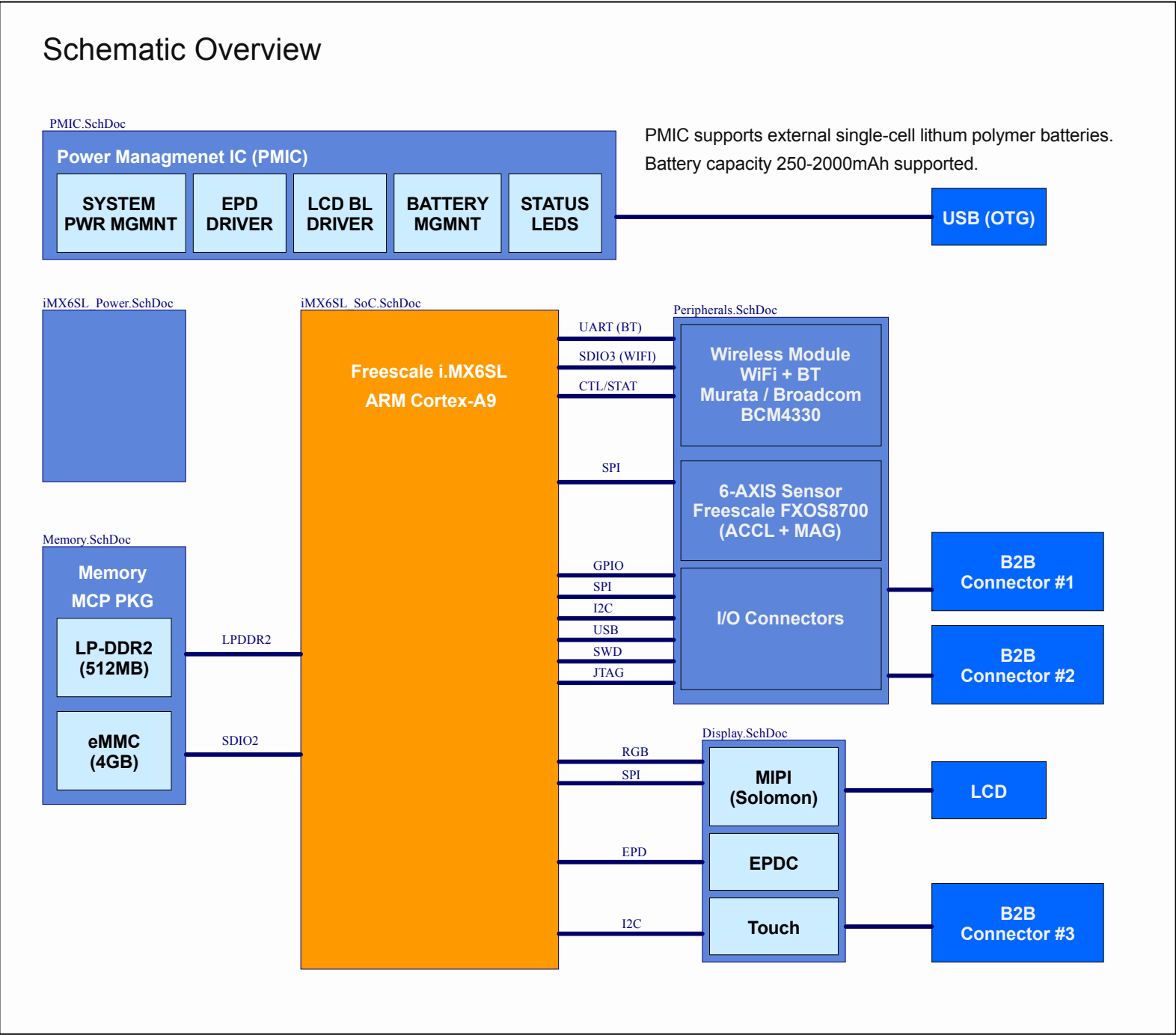


WaRP Mainboard Schematics

The Wearable Reference Platform (WaRP) has been developed in conjunction with Freescale, Kynetics, and Revotics. The hardware is designed by Revotics and is maintained and licensed under a Creative Commons Attribution-ShareAlike 4.0 International License. For the latest information, please visit our website at: <http://revotics.com/warp>



Document History

Date	Comment	Revision
01/15/2015	Initial Public Release	v1.11



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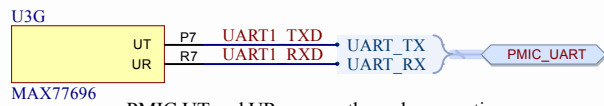
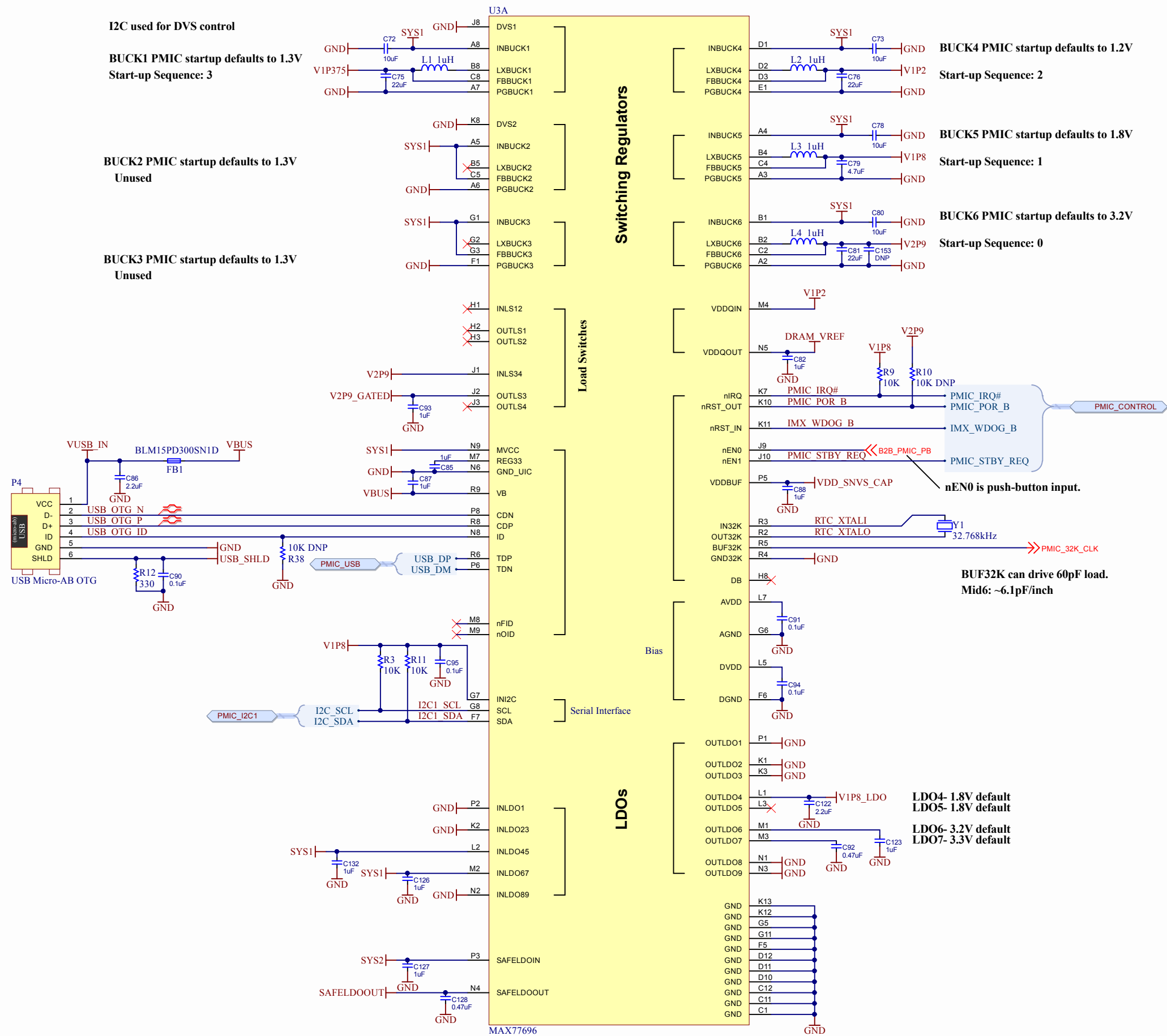
Project Name WaRP Mainboard			
Title Overview	Revision v1.11	Author Revolution Robotics, Inc. revotics.com Please visit our site for support and additional info.	
Filename: SystemLevelBlocks.SchDoc			
Date: 1/14/2015	Sheet Number: 1 of 7		

I2C used for DVS control

BUCK1 PMIC startup defaults to 1.3V
Start-up Sequence: 3

BUCK2 PMIC startup defaults to 1.3V
Unused

BUCK3 PMIC startup defaults to 1.3V
Unused



PMIC UT and UR are passthrough connections

PMIC Output Connections		
V1P375V - 1400mA		
VDD_ARM	1100mA	iMX6SL
VDD_SOC	650mA	iMX6SL
VDD_PU	150mA	iMX6SL
V1P2V - 610mA		
NVCC_DRAM	400mA	iMX6SL
VDD2 + VDDCA	???	LPDDR2
V1P8V - 800mA		
NVCC_18IO	400mA	iMX6SL
VDDIO	3mA	FXOS8700
VDD1	???	LPDDR2
VBBB 2P9V - 415mA		
NVCC_33IO	30mA	iMX6SL
VNVS	30uA	iMX6SL
VDD	3mA	FXOS8700
VCCQ + VCC	???	eMMC

LDO89 will leak 250uA if enabled via software.

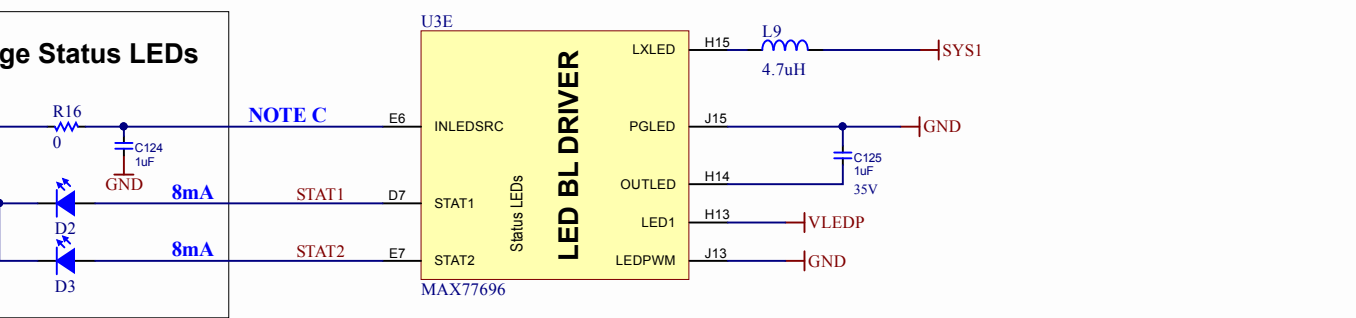
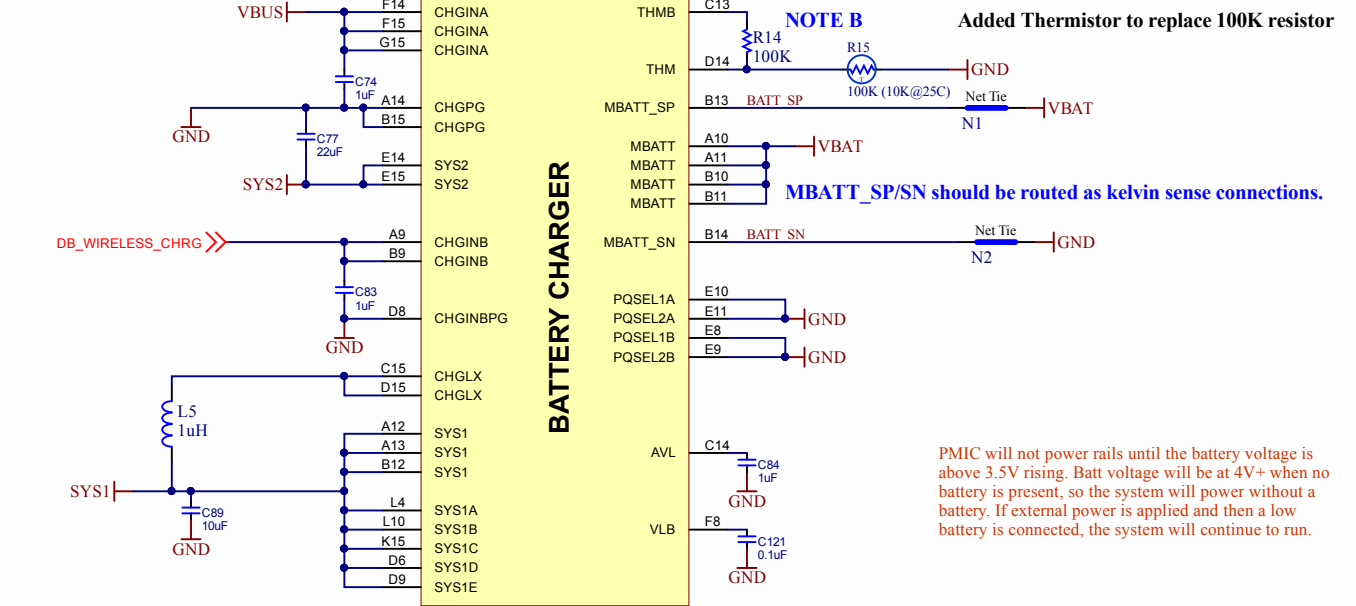
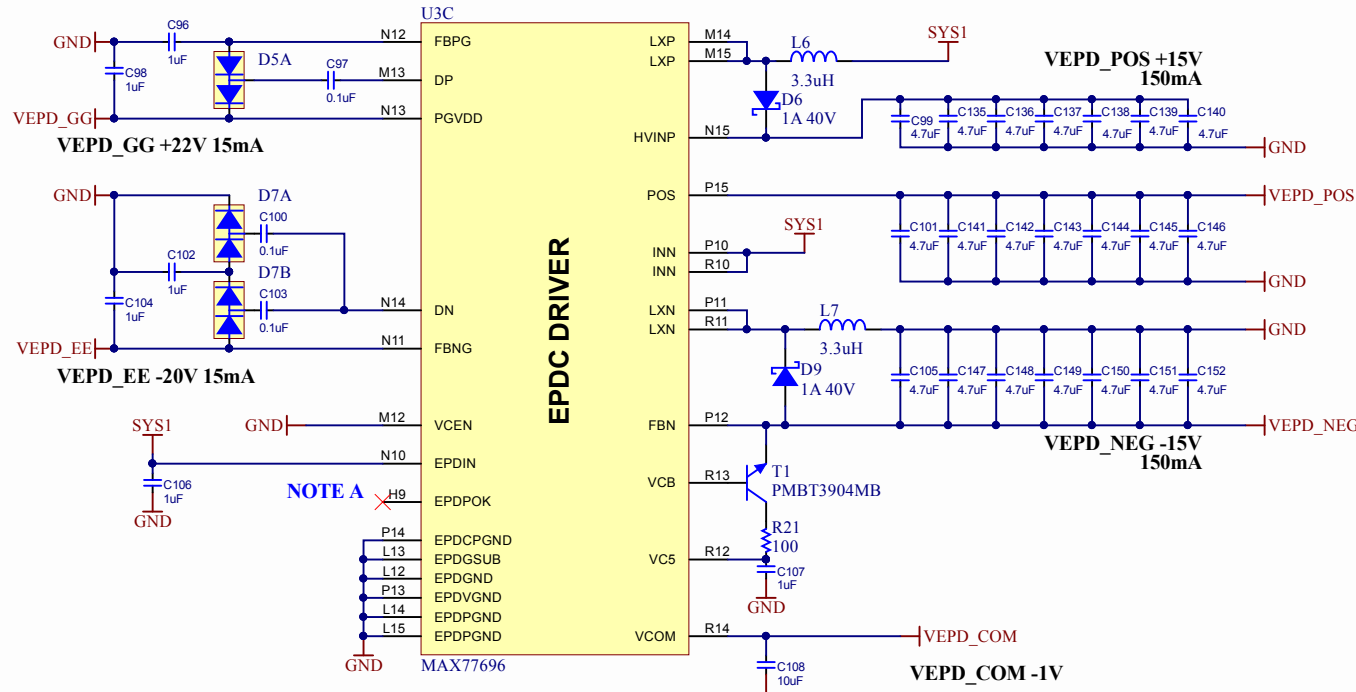
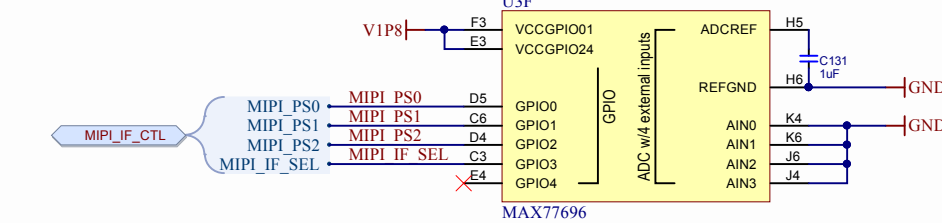
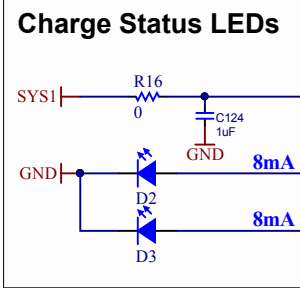
Total effective capacitance on BUCK5 outputs should be <18.8uF (see worksheet).

SYS2/CHNGINA provide reverse boost functionality for 5V/accessory power.

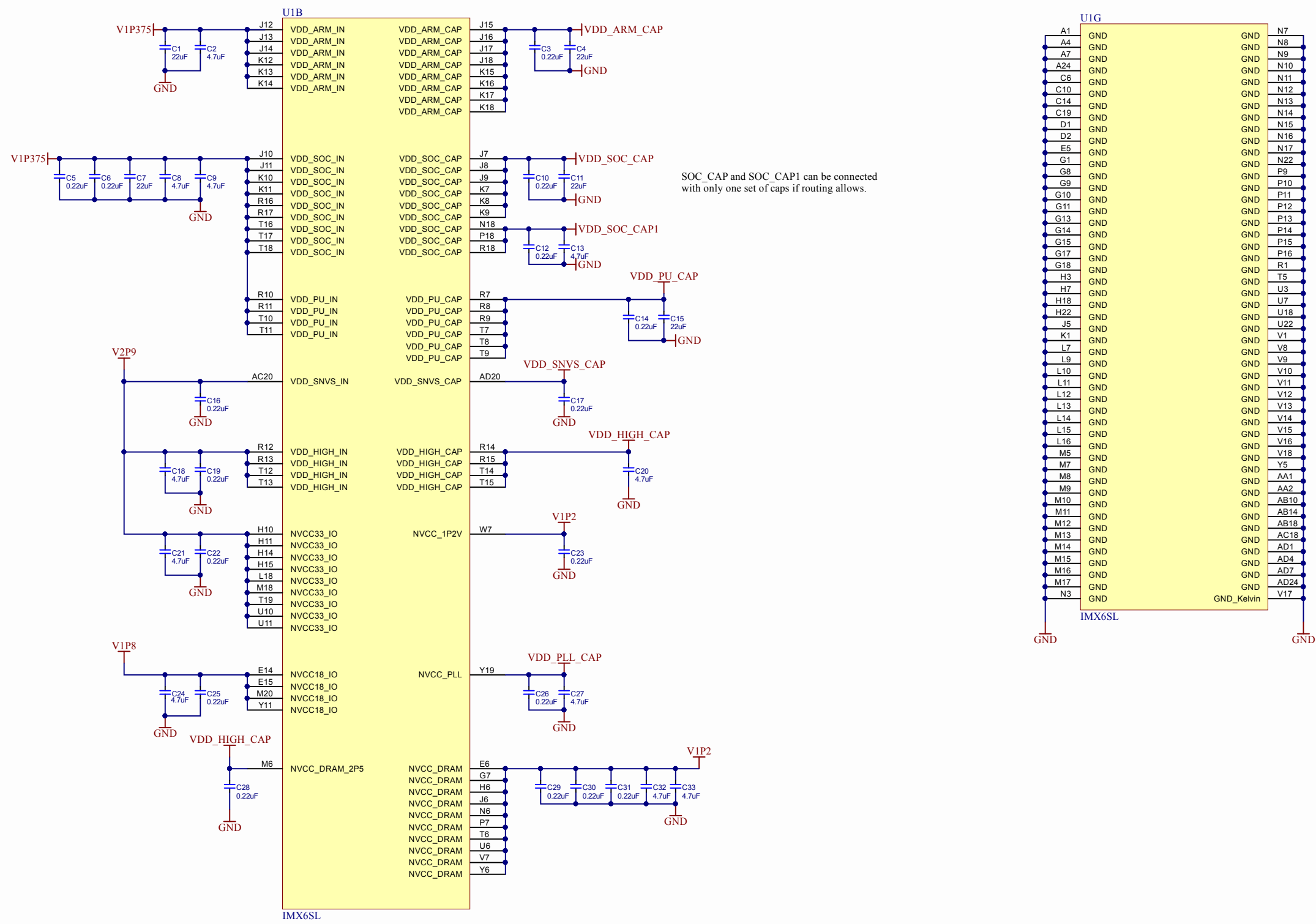
NOTE A. VCEN is internally OR'd with I2C register. Tie to GND and read EPDPK status from I2C.

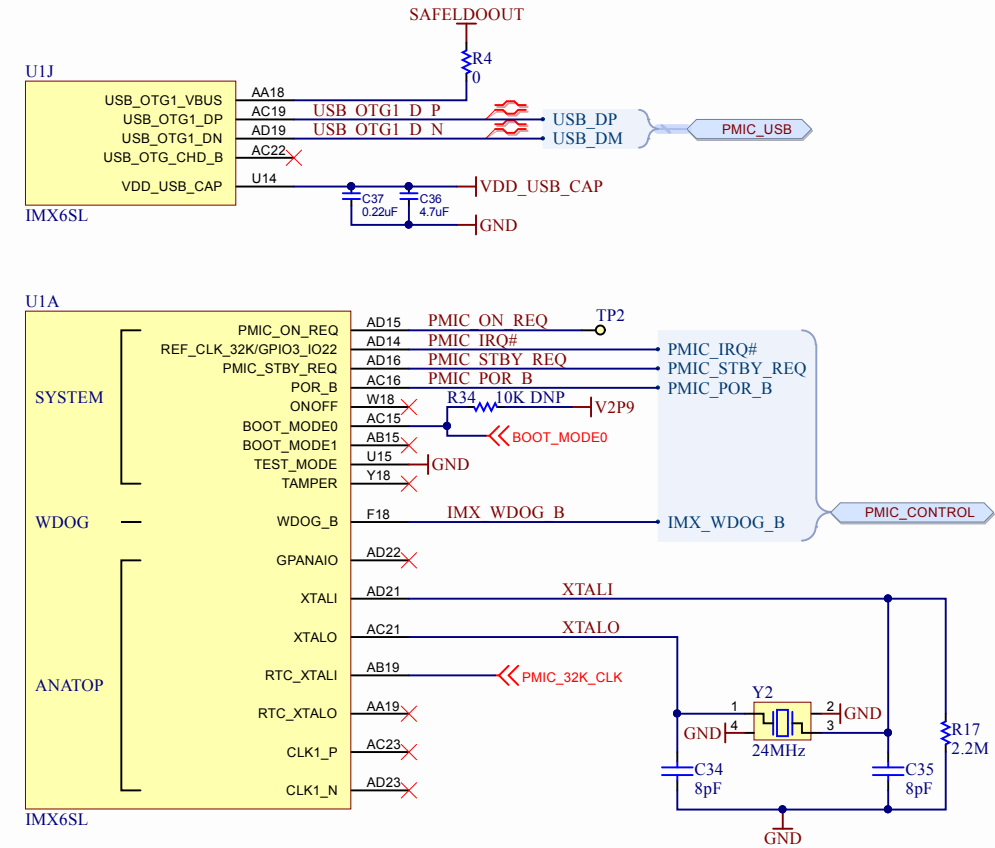
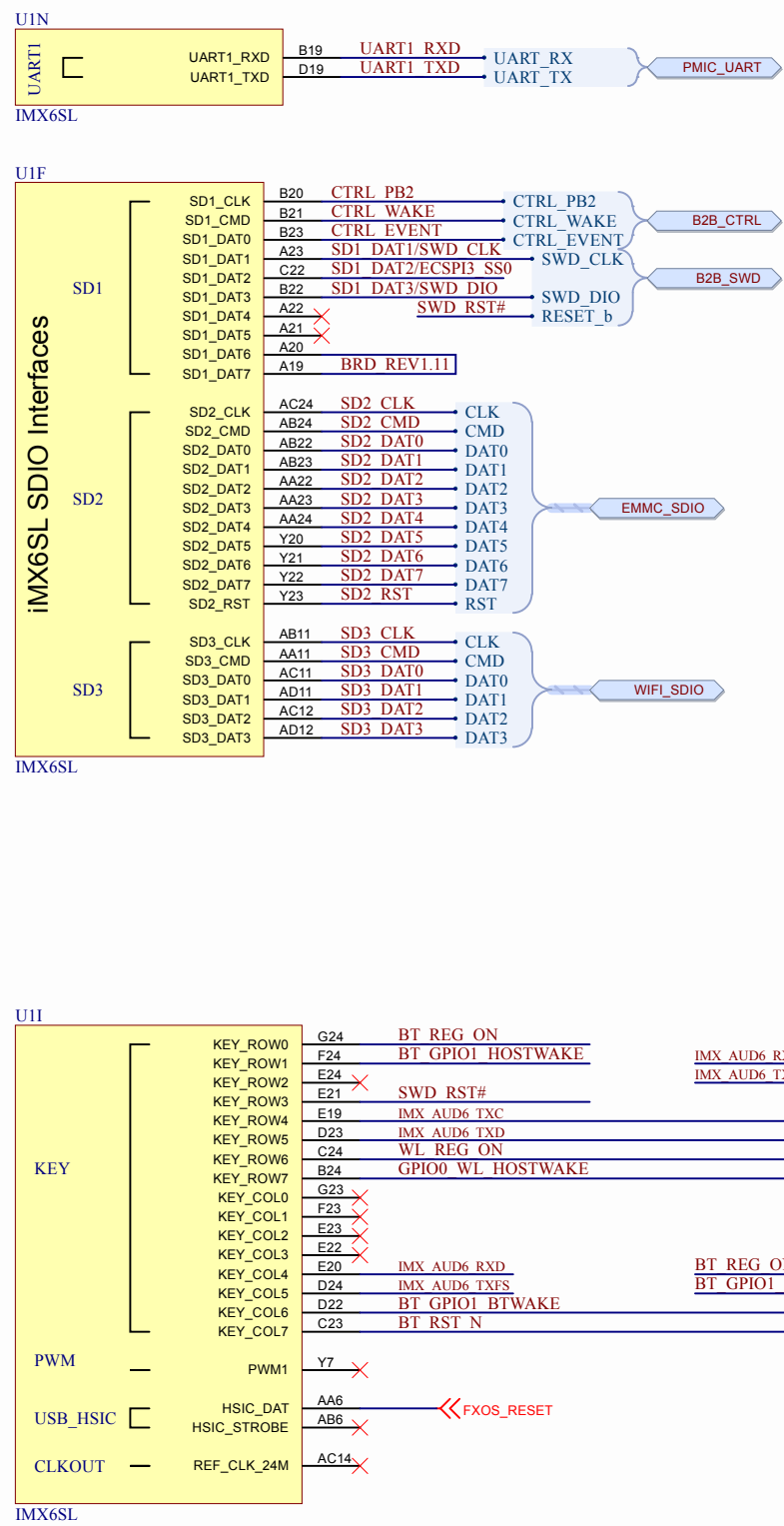
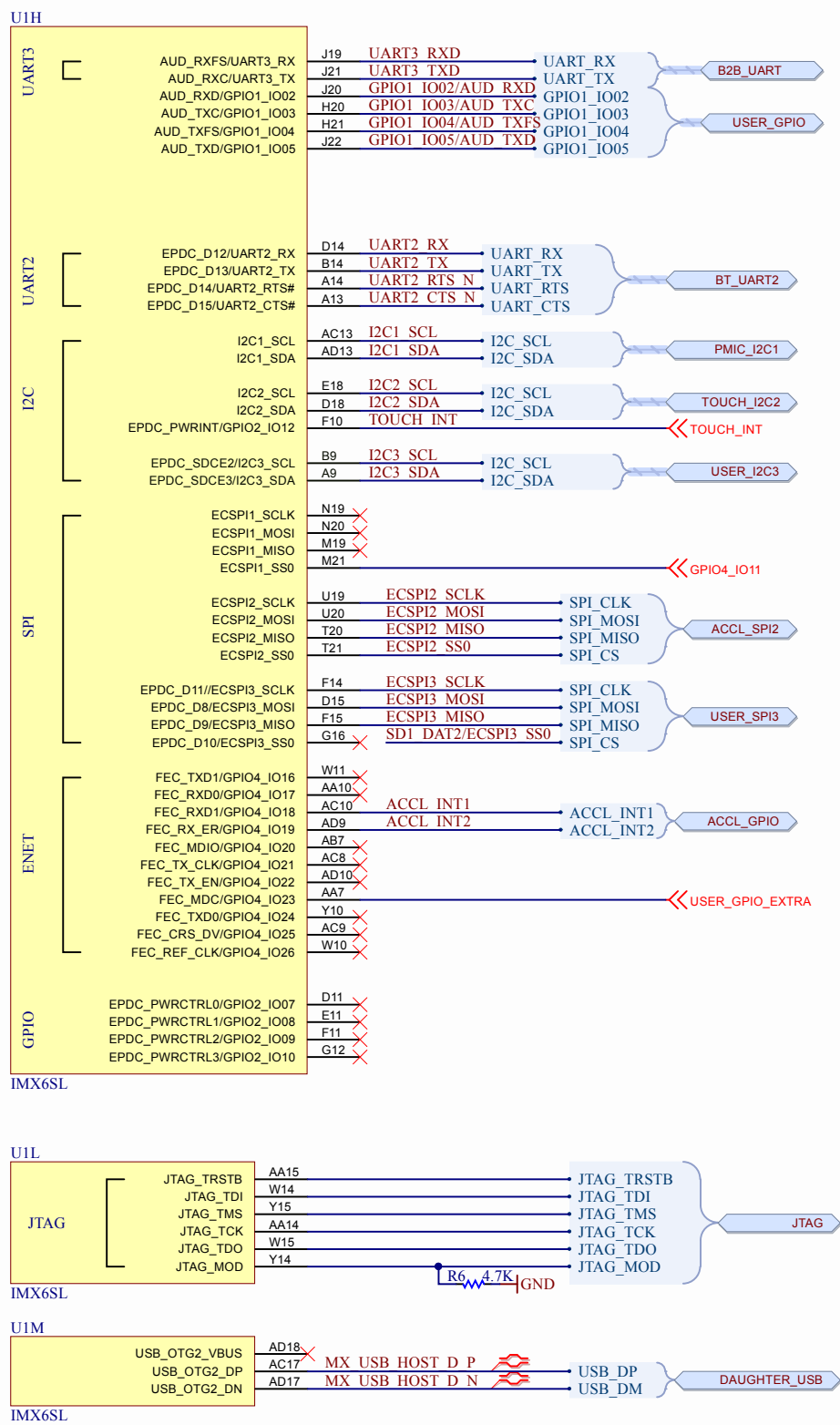
NOTE B. Terminate THM 100k to GND and 100k to THMB to bias temp reading to safe level in fuel gauge algorithm. Set the JEITA bit to 0 to not use THM in the charging algorithm.

NOTE C. Status LEDs on dev board only. For Final board, connect INLEDSRC to GND. For Dev board, C124 can be used as resistor pad to GND input if R16 is depopulated.

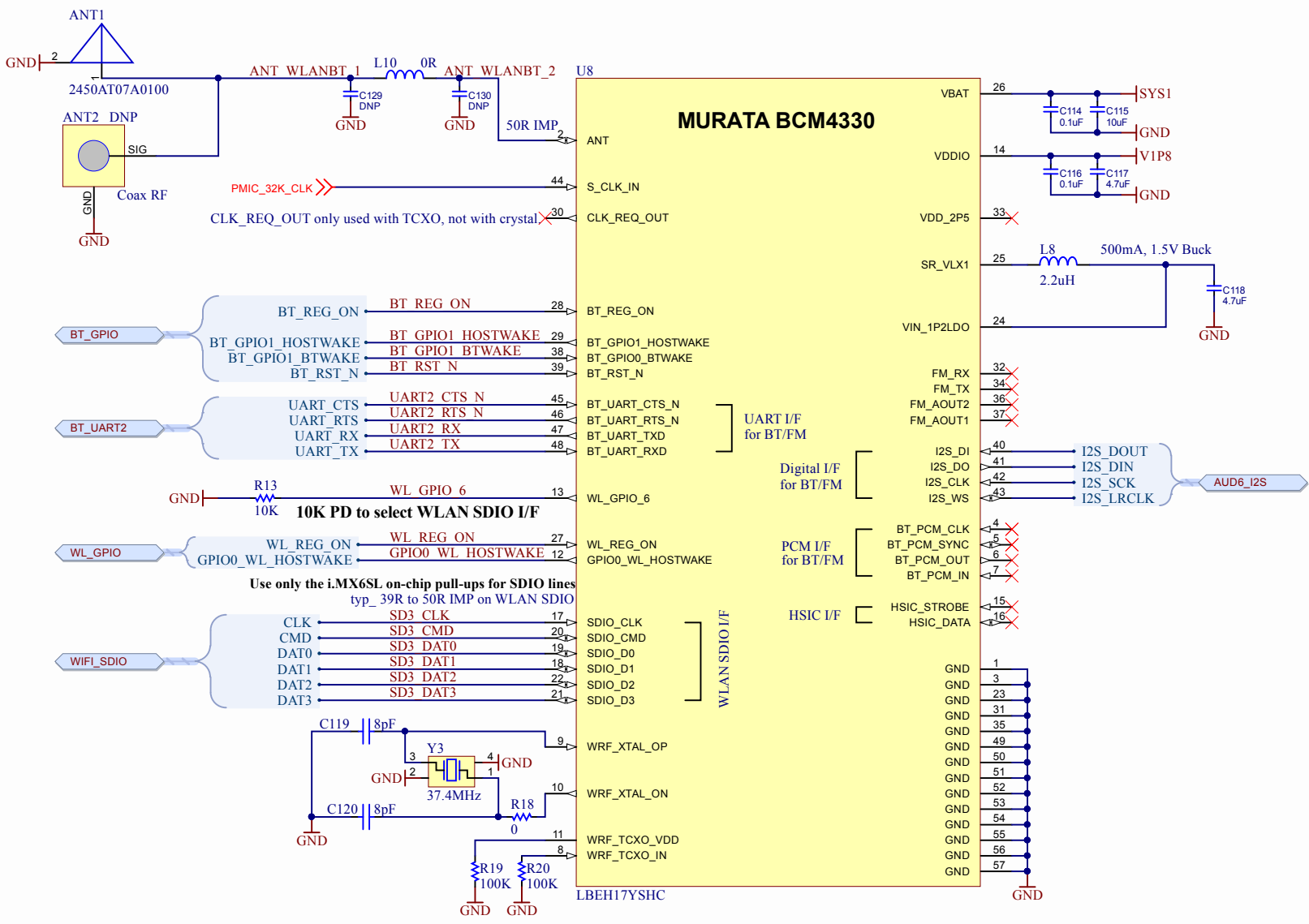


Project Name WaRP Mainboard		
Title PMIC	Revision v1.11	Author Revolution Robotics, Inc. revotics.com
Filename: PMIC.SchDoc	Date: 1/14/2015	
Sheet Number: 2 of 7		Please visit our site for support and additional info.





Wireless



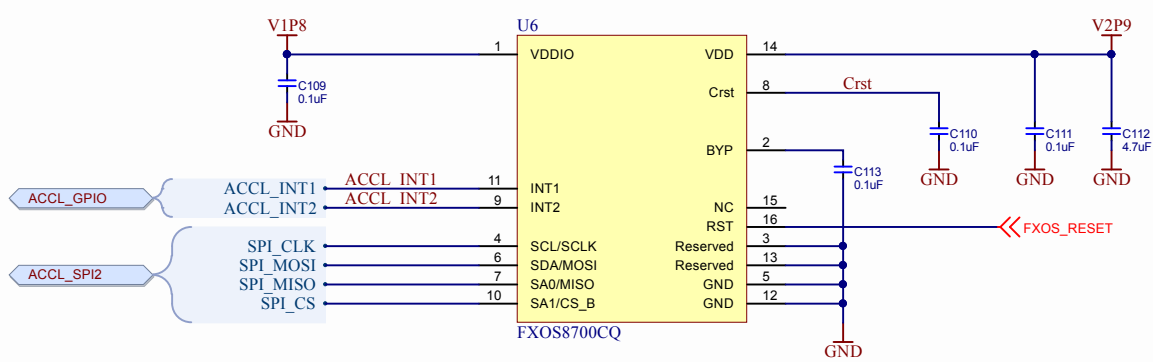
R18 Typical value listed as 0-330 dependent upon crystal.
Value may need optimization.

WLAN GPIO strapping options for WLAN I/F selection

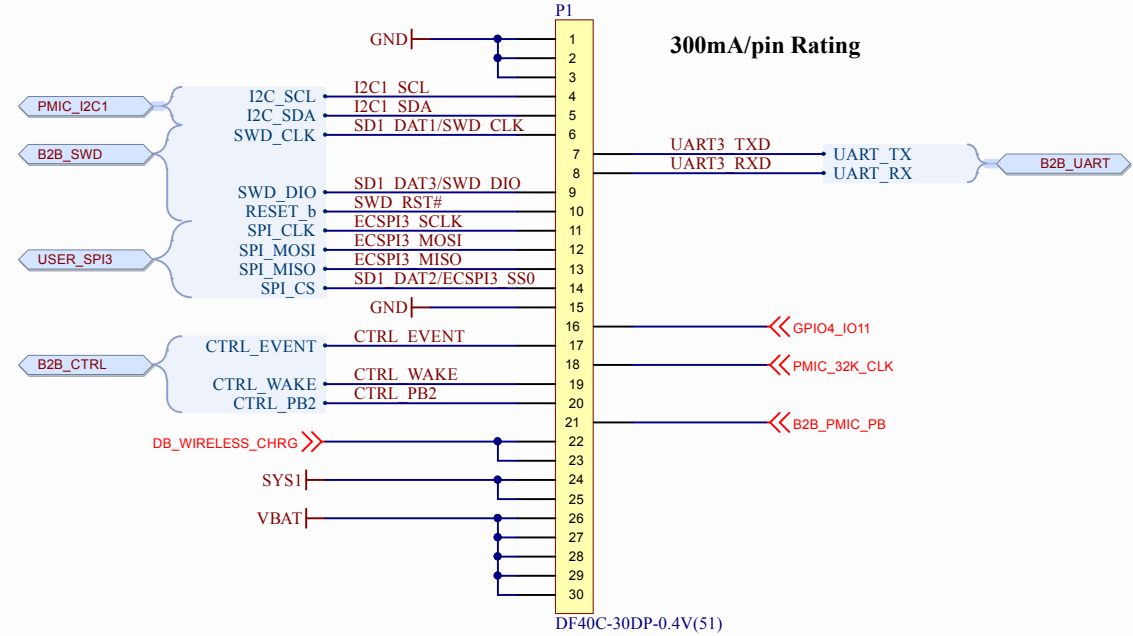
WL_GPIO 6	SDIO D2	SDIO D1	Interface
PullDN	---	---	SDIO
PullUP	PullDN	---	SPI
PullUP	PullUP	PullDN	Normal HSIC
PullUP	PullUP	PullUP	Bootloader-less HSIC

Resistor size is 10kOhm or less for each setting.

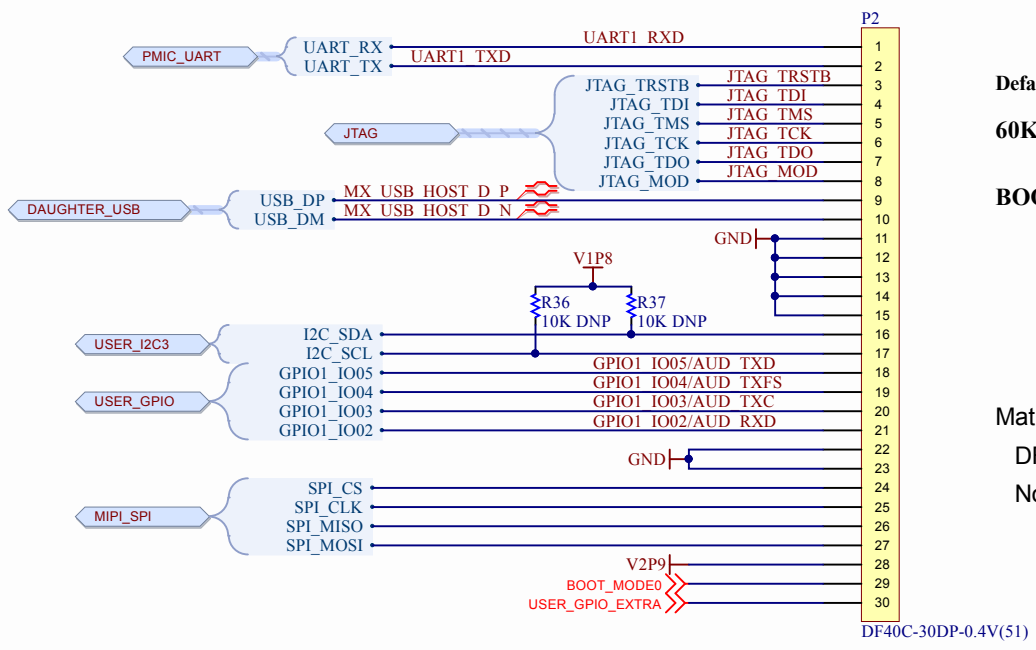
FXOS8700 Accelerometer



Daughterboard Connector (Port 1)



Mechanical/Debug Connector (Port 2)



See the Displays schematic page for the 3rd I/O connector (Port 3)

Default BOOT MODE jumpers should be added to mainboard

60KO-140KO Internal PD on iMX6SL

00 - Boot from fuses

BOOT_MODE[1:0] 01 - Serial Downloader

10 - Internal Boot (Development)

Mating connector to use on Daughterboard:
DF40HC(3.0)-30DS-0.4V(51)

Note: Work with all height variants (dependent only on DB)